Optimization of Photonic Soldering Processes for SIR Performance

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Abstract
Photonic soldering is a reflow process wherein solder, pads, and components are heated by high-intensity, pulsed light from a flash lamp. Typical cycle times for a photonic soldering process are in the range of several seconds, requiring drastically less energy consumption than a convection reflow oven for a wide range of standard solder alloys. While these short cycle times are typically regarded as an advantage for process throughput [1-3], it is critical to also consider their implications on other aspects of the reflow process. This work considers surface insulation resistance (SIR), a critical metric for reliability performance, which is derived primarily from the flux residue remaining on a printed circuit board (PCB) after reflow. An in-line photonic soldering tool is used to reflow two no-clean, Pb-free, Type 4 SAC305 paste formulations on IPC B-24 test coupons across a range of different settings. The results of this study highlight the role of two parameters unique to photonic soldering – average radiant power and cumulative radiant exposure – in developing a process qualified for SIR performance. This investigation shows how these parameters may be adjusted to improve SIR, in a manner analogous to the development of a standard temperature profile for oven reflow. Additionally, this study demonstrates the successful reflow of a low-residue paste, originally developed for an inert atmosphere, using the photonic soldering approach with ambient air. These findings indicate compelling new possibilities for solder paste chemistry that leverage the unique characteristics of photonic soldering.

Introduction
Surface insulation resistance (SIR) is a key qualification parameter for soldering processes. It pertains to two reliability concerns in assembled printed circuit boards (PCBs): current leakage, and electrical shorting via dendritic growth. Even in PCBs assembled with well-qualified paste and under optimized reflow conditions, nonzero current leakage across neighboring traces is possible [5-6]. In such cases, the majority of current leakage is mediated by flux residues that remain on the PCB surface after reflow. Similarly, dendrite formation, driven by an electrical bias across adjacent traces, is also facilitated by flux residues that seep into the areas between traces. SIR is therefore an indicator of device performance and reliability with respect to these two failure mechanisms [5-7].

Many commercially available solder pastes specify an SIR test standard [7-8]. Many of these test standards, including the widely used J-STD-004 from IPC, comprise periodic measurements across interdigitated copper traces, subjected to a steady electrical bias, under elevated temperature and humidity conditions [7]. Generally, ensuring that SIR performance meets or exceeds a standard threshold is integral to the development of commercial paste formulations. However, SIR performance also depends on a well-optimized assembly process, which is why official product datasheets generally include a recommended reflow profile. Recommendations for one process – temperature profiles for reflow ovens are the most common – do not always translate directly to other methods of reflow. Thus, when developing a new reflow process for an existing solder paste system, it is essential to optimize SIR performance. Towards this effort, a fundamental understanding of physical mechanisms related to reflow is greatly beneficial.

Photonic soldering is a thermal process that achieves heating in a fundamentally different way than other established reflow methods. Photonic processing techniques apply intense, broad-spectrum visible light over a large area. The operative heat transfer mode is radiation, rather than convection or conduction [1-3]. Commercially available photonic soldering tools can achieve radiant output intensity as high as 70 $W \cdot cm^{-2}$, and in practice, this output is typically modulated by pulsing the light source [9]. The result is non-contact heating that is simultaneously rapid and precise. In contrast to oven reflow, photonic soldering is a non-equilibrium thermal process [10]. The high rate of heat transfer involved ensures that flux activation and alloy melting are completed prior to temperature equilibration throughout the PCB. Additionally, the difference in optical absorption of the various materials that compose the PCB results in a selective heating mechanism. It is typical for the solder paste and pads to be the most optically absorptive materials on a PCB, and thus the local heating rate is highest at areas of the PCB layout where heat is desirable [3].

The standard process recipe for photonic reflow comprises two physical parameters: average radiant power, and cumulative radiant exposure. These can be specified in units of $W \cdot cm^{-2}$ and $J \cdot cm^{-2}$, respectively. This process space represents another key

distinction from convection oven reflow, which instead specifies temperature profiles comprising set points, ramp rates, and durations for specific profile segments. While photonic soldering processes can be characterized in terms of temperature, energy profiles are commonplace since they are more convenient to implement directly. It is important to note that since photonic soldering is a non-equilibrium heating method [10], it produces different temperature profiles at different locations on the board. For example, peak temperatures are generally reduced near the side of the PCB facing away from the photonic source. Thus, it is far more practical to define a photonic reflow process in terms of incident energy, which is uniform across the PCB, rather than temperature.

With respect to SIR, one of the most consequential aspects of photonic soldering is its extremely short cycle time. Only a few seconds or less are required for reflow in photonic soldering processes [1-3, 9-12], in contrast to convection oven reflow, which generally requires several minutes for a full cycle [13-14]. This rapid process speed is frequently cited purely as an advantage, by virtue of increased throughput. However, the reality is more nuanced. The abbreviation of process time afforded by photonic soldering affects multiple physical processes associated with reflow. These physical processes include flux activation implementation of oxide cleaning at pads, contact line movement of molten solder, evaporation of volatile flux constituents, and further oxidation of metal surfaces at elevated temperatures [13-14]. Each of these is relevant to the final SIR performance in an assembled PCB.

In this work, SIR is measured for solder paste reflowed using a photonic process, and guidelines are developed for optimizing SIR performance of PCBs assembled using photonic reflow. While previous studies on photonic soldering have optimized process conditions with respect to solder junction quality [9-12] and process yield [3], the present study is the first so far to consider SIR. The scope of this work encompasses two commercially available Pb-free no-clean solder pastes: one general-purpose formulation, and one low-residue formulation that requires <100 ppm O_2 for convection oven reflow. IPC-TM-650-compliant test coupons are assembled with either of these two paste formulations using a range of photonic processing conditions, and the resulting SIR performance is characterized using the IPC J-STD-004B protocol. The results are used to highlight considerations for SIR performance which are characteristic of photonic reflow processing, and to explain the influence of photonic process parameters on SIR. The results from this work also highlight some interesting possibilities for processing low-residue paste formulations in ambient atmosphere.

Experimental Methodology

Materials

The SIR performance evaluations in this study were carried out using two formulations of SAC305 type 4 solder paste. The first, paste "S", uses a ROL0 flux formulation, and is a general-purpose variety intended for either ambient air or low-oxygen atmospheric environments. The second, paste "LR" uses a low-residue REL0 flux formulation that requires <100 ppm O_2 atmosphere when processing using a convection oven. Both paste formulations are available commercially, and standard temperature profiles for oven reflow are available from the manufacturer. Neither paste formulation was originally developed for photonic reflow.

Two separate test coupons were used for the purposes of this study. Initial demonstrations of process viability were carried out using the coupon shown in Figure 1(a), which includes 0805 chip component pads arranged in a grid pattern. The construction of this test coupon is a 1.6 mm thick fiberglass-epoxy resin composite substrate, clad with 1 oz. (34.8 µm thick) copper signal layers on both top and bottom surfaces, with green solder mask and organic solderability preservatives (OSP) finish. For SIR characterizations, the IPC B-24 test coupon pictured in Figure 1(b) was used. The SIR test coupon construction is single-layer 1 oz. (34.8 µm thick) copper on 1.6 mm thick fiberglass-epoxy resin composite with no solder mask. Its layout comprises four functionally identical circuits, each of which can be used to measure SIR across interdigitated comb-shaped traces.

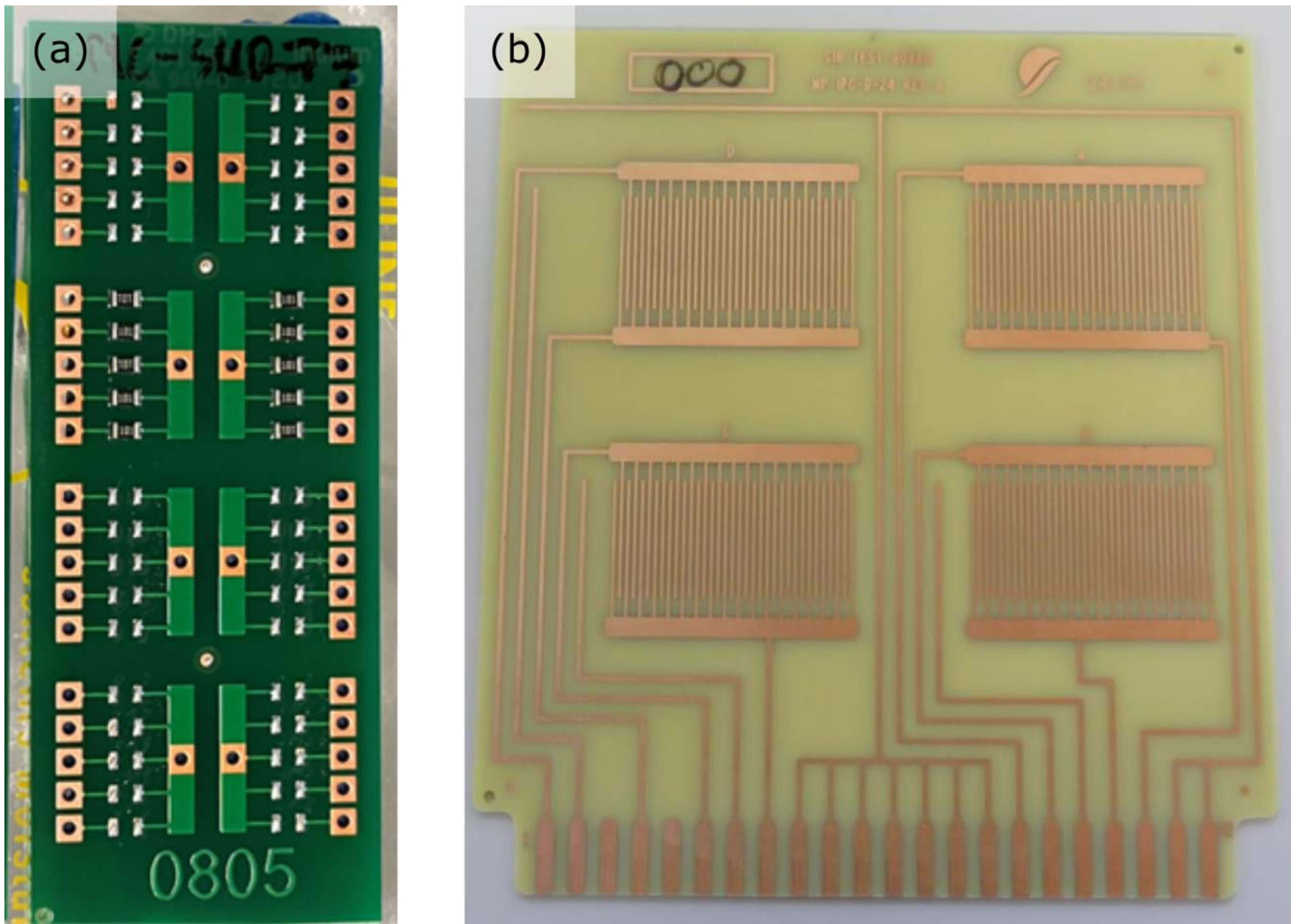

Figure 1. Images of the two types of test coupons used in this study, (a) an array of 0805 chip component pads and (b) an SIR test coupon compliant with IPC-TM-650.

Procedures

Prior to assembly, all test coupons were cleaned with isopropanol and de-ionized water, baked, and immediately moved to ESD-safe sealed packaging for storage. Test coupons were only removed from packaging immediately prior to assembly and processing. Paste printing of test coupons shown in Figure 1(a) was carried out by hand using a 102 µm thick, laser-cut, steel stencil. Paste printing on SIR test coupons pictured in Figure 1(b) was carried out on an automatic stencil printer, ESE model US-X2000, using a 127 µm thick laser-cut steel stencil and steel squeegee angled at 60°. Placement of chip resistors on the test coupons shown in Figure 1(a) was carried out by hand.

Photonic processing was carried out using a PulseForge® model FX4-52-30 In-Line photonic soldering tool, operated in ambient atmosphere. For initial demonstrations of process viability, the test coupons shown in Figure 1(a) were processed with a cumulative radiant exposure of 88 J·cm^{-2}, an average radiant power of 22 W·cm^{-2}, and a radiant exposure per pulse of 0.5 J·cm^{-2}. These parameters were achieved using a pulse frequency of 44 Hz and pulse count of 176 per unit area, with a bank voltage of 480 V and individual pulse window of 490 µs. These conditions were chosen to ensure full reflow at all solder pads with good wetting.

For IPC B-24 test coupons shown in Figure 1(b), four different photonic soldering conditions were used to reflow each of the two solder paste formulations. For all conditions, individual photonic pulses were shaped with a bank voltage of 480V and a pulse window of 490 µs, and the remaining process settings are organized in Table 1 and Table 2 for solder paste "S" and solder paste "LR", respectively. Under conditions 1A and 1B (described in Table 1 and Table 2 respectively), test coupons sustained a relatively low cumulative radiant exposure, registering near the minimum value observed to yield complete reflow and good wetting. Conditions 2A and 2B (also described in Table 1 and Table 2 respectively) represent a relatively high cumulative radiant exposure, near the onset of cosmetic damage and discoloration to copper traces and laminate material. In all other respects, conditions 2A and 2B were identical to 1A and 1B, respectively. The remaining conditions in Table 1 and Table 2 added an additional process cycle after reflow. In consideration for the extremely short process time relative to convection oven reflow, the method for which these pastes were originally developed, the second process cycle used for

131 conditions 3A, 3B, 4A and 4B (described in Table 1 and Table 2) were included with the intent to remove residual solvents
132 from the flux residue without surpassing the melt temperature of the SAC305 alloy. For conditions 3A and 3B, the duration of
133 the second process cycle was the same as for conditions 2A and 2B, respectively. For conditions 4A and 4B, the duration of
134 the second process cycle was extended to 10 seconds, with the same cumulative radiant exposure as with conditions 3A and
135 3B.
136
137 **Table 1. Process conditions used for photonic reflow of IPC B-24 test coupons printed with solder paste "S" for**
138 **characterization of SIR performance.**
139

Photonic condition	Process cycle 1[a]		Process cycle 2[a]	
	Cumulative radiant exposure (J·cm^{-2})	Average radiant power (W·cm^{-2})	Cumulative radiant exposure (J·cm^{-2})	Average radiant power (W·cm^{-2})
1A	80	23		
2A	105	30		
3A	105	30	63	18
4A	105	30	63	6.2

140
141
142 **Table 2. Process conditions used for photonic reflow of IPC B-24 test coupons printed with solder paste "LR" for**
143 **characterization of SIR performance.**
144

Photonic condition	Process cycle 1[a]		Process cycle 2[a]	
	Cumulative radiant exposure (J·cm^{-2})	Average radiant power (W·$^{-2}$)	Cumulative radiant exposure (J·cm^{-2})	Average radiant power (W·cm^{-2})
1B	88	22		
2B	105	26		
3B	105	26	63	16
4B	105	26	63	6.2

145
146 Chip component test coupons were embedded in an acrylic mold compound for cross-sectioning. After grinding and polishing,
147 these samples were characterized using an AxiaTM ChemiSEMTM scanning electron microscope (SEM).
148
149 IPC B-24 test coupons were placed in an environmental test chamber at 40°C and 90% relative humidity for SIR testing. Surface
150 insulation resistance was monitored for 168 hours according to IPC test protocol IPC-TM-650 2.6.3.7.
151
152 **Results**
153 *Process Viability*
154 To confirm the viability of photonic reflow for assembly of electronic circuits with both solder paste types used in the present
155 study, 0805 chip resistors were assembled on the test coupon shown in Figure 1(a). SEM images of the resulting solder junctions
156 are shown in cross-section in Figure 2. The overall fillet structure for chip components attached with solder paste "S" and "LR"
157 are shown in Figure 2(a) and Figure 2(b), respectively. These cross-section images exhibit complete reflow, well-formed
158 menisci, and low contact angles at both the component and resistor pads.
159
160 The metallurgical structure of solder paste "S" and solder paste "LR" post-reflow are shown at higher magnification in Figure
161 2(c) and Figure 2(d), respectively. For both solder pastes, complete solder adhesion at all pads and formation of intermetallic
162 compound (IMC) is evident. The IMC regions for both pastes exhibit a regular scalloped shape, ranging from about 1-2µm in
163 thickness at most points, and with low voiding. Paste "S" and paste "LR" exhibit very little difference in overall metallurgical
164 structure, and those differences that do exist, such as component stand-off height, are attributable to manual component
165 placement and paste deposition using a hand stencil. In summary, photonic reflow produces acceptable solder junctions for
166 components assembled using both solder pastes considered in this study. Furthermore, there were no distinguishable differences
167 in junction morphology resulting from the choice of paste chemistry.
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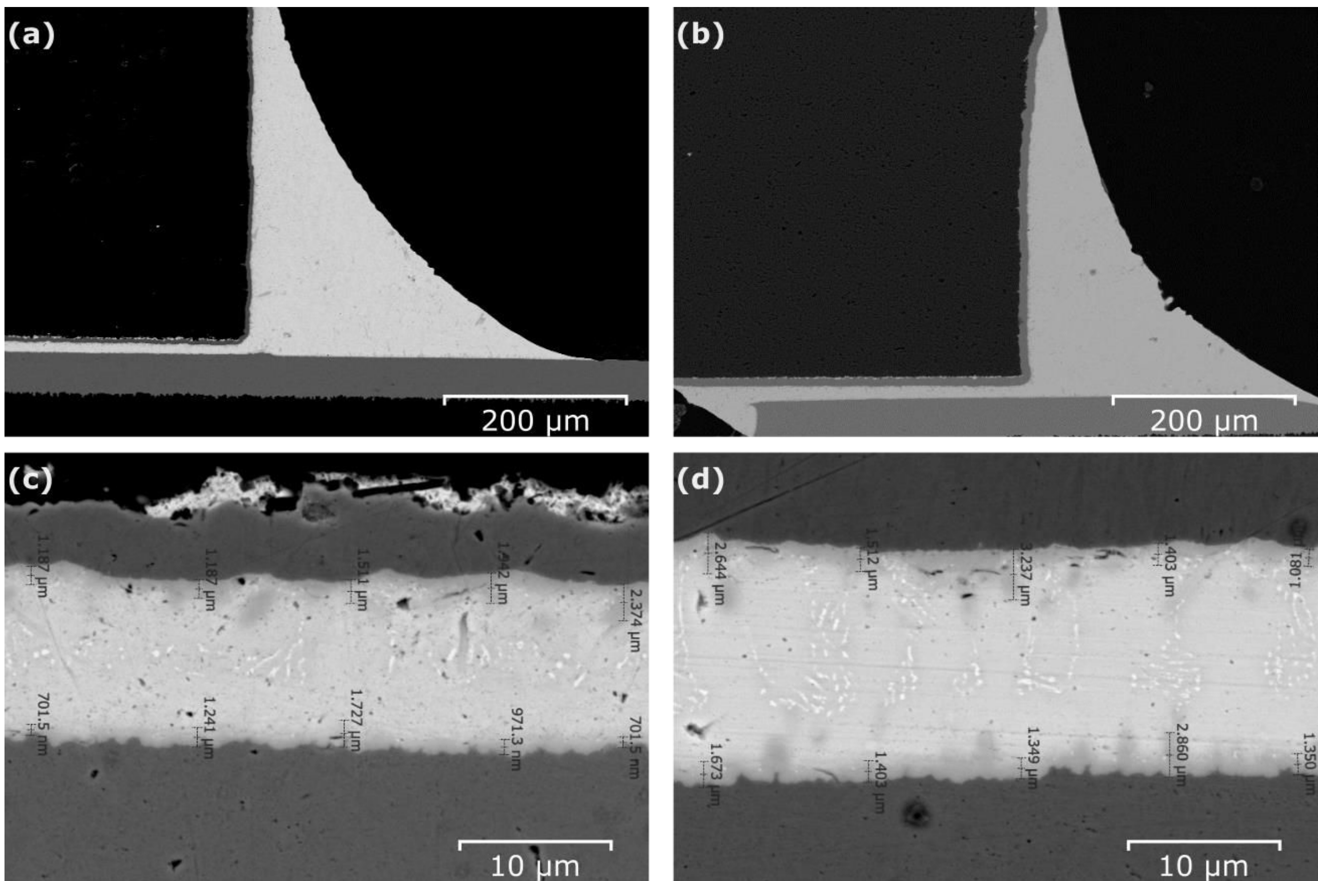

Figure 2. Scanning electron microscopy of 0805 chip resistors assembled using photonic reflow. Views of the meniscus structure of solder paste "S" and solder paste "LR" are shown in (a) and (b), respectively. Detail views of the metallurgical grain structure are shown for solder paste "S" and solder paste "LR" in (c) and (d), respectively.

The result shown in Figure 2(b) and Figure 2(d) is particularly noteworthy because the reflow processing step was carried out in ambient air, whereas solder paste "LR" requires a low-oxygen environment (<100 ppm O_2) for convection oven reflow. The expected behavior of this paste for oven reflow in ambient air is severe de-wetting and beading initially, and ultimately the absence of consistent metallurgical bonds over the pad areas. The same behavior is expected for many other flux products, available from a wide variety of manufacturers, which specify inert or low-oxygen atmosphere as a requirement for reflow processing. While these fluxes are capable of cleaning existing oxides from the surfaces of pads, they are not designed to remove large amounts of additional oxide introduced during the reflow step. This is what motivates the low-oxygen atmosphere requirement for various commercial fluxes, which ensures that the supply of oxygen is limited. Photonic reflow, however, is capable of introducing a rate restriction on oxide formation. In turn, this rate restriction reduces the level of oxide removal required from the flux in order to ensure good solder wetting and adhesion.

Standard Commercial Paste

Figure 3 summarizes the influence of photonic processing conditions on SIR performance of solder paste "S", as measured according to J-STD-004B with test coupon IPC B-24. Comparing the results for photonic conditions 1A and 2A in Figure 3(a) and Figure 3(b), respectively, it is apparent that cumulative radiant exposure – i.e. the total radiative energy output from the full duration of the photonic process – is influential in the final SIR performance. Whereas the results in Figure 3(a) fall well below the 10^8 Ω requirement from IPC J-STD-004B, the performance shown in Figure 3(b) is merely borderline, with measured SIR at several channels surpassing the 10^8 Ω minimum value, and the average across all channels slightly above that threshold. By contrast, the additional process cycles added for photonic conditions 3A and 4A do not appear to have any appreciable effect on SIR performance. The results for condition 3A, shown in Figure 3(c), exhibit a marginally lower average and narrower data range across all channels compared to the results from Figure 3(b). Similarly, the results for condition 4A, shown in Figure 3(d), exhibit a marginally higher average and wider data range compared to the Figure 3(b) results. These marginal differences are not large enough to distinguish easily from the overall variability within the data set.

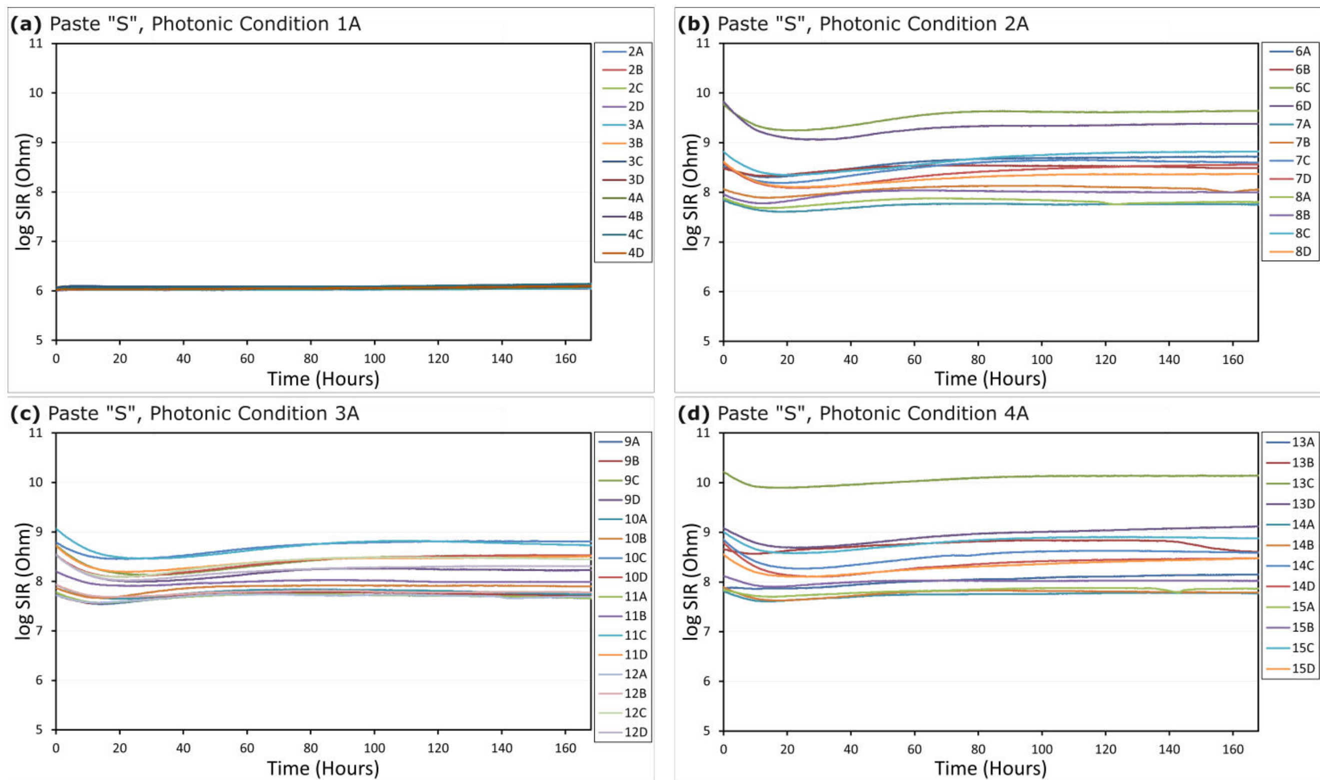

Figure 3. Summary of SIR results for test coupons printed with paste "S" and processed using (a) photonic condition 1A (b) photonic condition 2A, (c) photonic condition 3A, and (d) photonic condition 4A. Each data series corresponds to a specific SIR test coupon circuit, with four circuits per test coupon. The legend labels of each subplot are the unique identifiers for these circuits.

Recalling the cross-sections from Figure 2(a) and Figure 2(c), solder paste "S" is known to exhibit complete reflow, wetting, and IMC formation when processed with photonic parameters similar to condition 1A. Thus, it is unlikely that the differences in SIR performance among the four data sets plotted in Figure 3 relate to either oxide removal or cleaning activity at pad surfaces. Instead, the results shown in Figure 3 reflect differences in either the flux residue composition, distribution, or both.

If it is flux residue composition that accounts for the final SIR performance of the coupons processed with solder paste "S", then differences among the four data sets shown in Figure 3 reflect differences in the efficacy of removal of volatile compounds from the flux vehicle during reflow. Comparing the improvement in SIR performance for conditions 2A, 3A and 4A relative to condition 1A, and the negligible effect of the second process cycle used for conditions 3A and 4A, it seems that removal of volatile compounds from the flux vehicle is far more effective at temperatures above the melting point of the solder alloy than at temperatures closer to the onset of flux activation. It is also possible that the second process cycles within condition 3A and condition 4A do change the flux residue composition to some degree, but the rate of change is sufficiently slow compared to the process time that the SIR performance does not change by a measurable amount.

The other possible cause for differences in SIR performance is the distribution of flux residue. To examine this possibility, Figure 4 shows top-down microscope images of the SIR test coupons after processing. For all four process conditions, solder coverage along the interdigitated fine traces of the test coupons is complete, without visible pinholes, bulges, or other wetting-related defects. This corroborates the previous results from Figure 2(a) and Figure 2(c), which exhibit low contact angles that are characteristic of favorable wetting. Nevertheless, in Figure 4, the bus bar features of the test coupon layout appear to be largely solder-free. It should be noted that the bus bar features do not receive paste coverage during the printing step, in contrast to the interdigitated fine traces, where paste is deposited directly. For the test coupon in Figure 4(a) processed under photonic condition 1A, the solder contact line exhibits minimal displacement beyond the stencil print area. For the remaining test coupons in Figure 4(b)-(d), several millimeters of solder contact line advancement beyond the original stencil print boundary are evident. Both the extent and irregular shape of the contact line advancement is comparable across all three test coupons in Figure 4(b)-(d), which reflects the commonality in reflow process cycle settings across conditions 2A, 3A, and 4A.

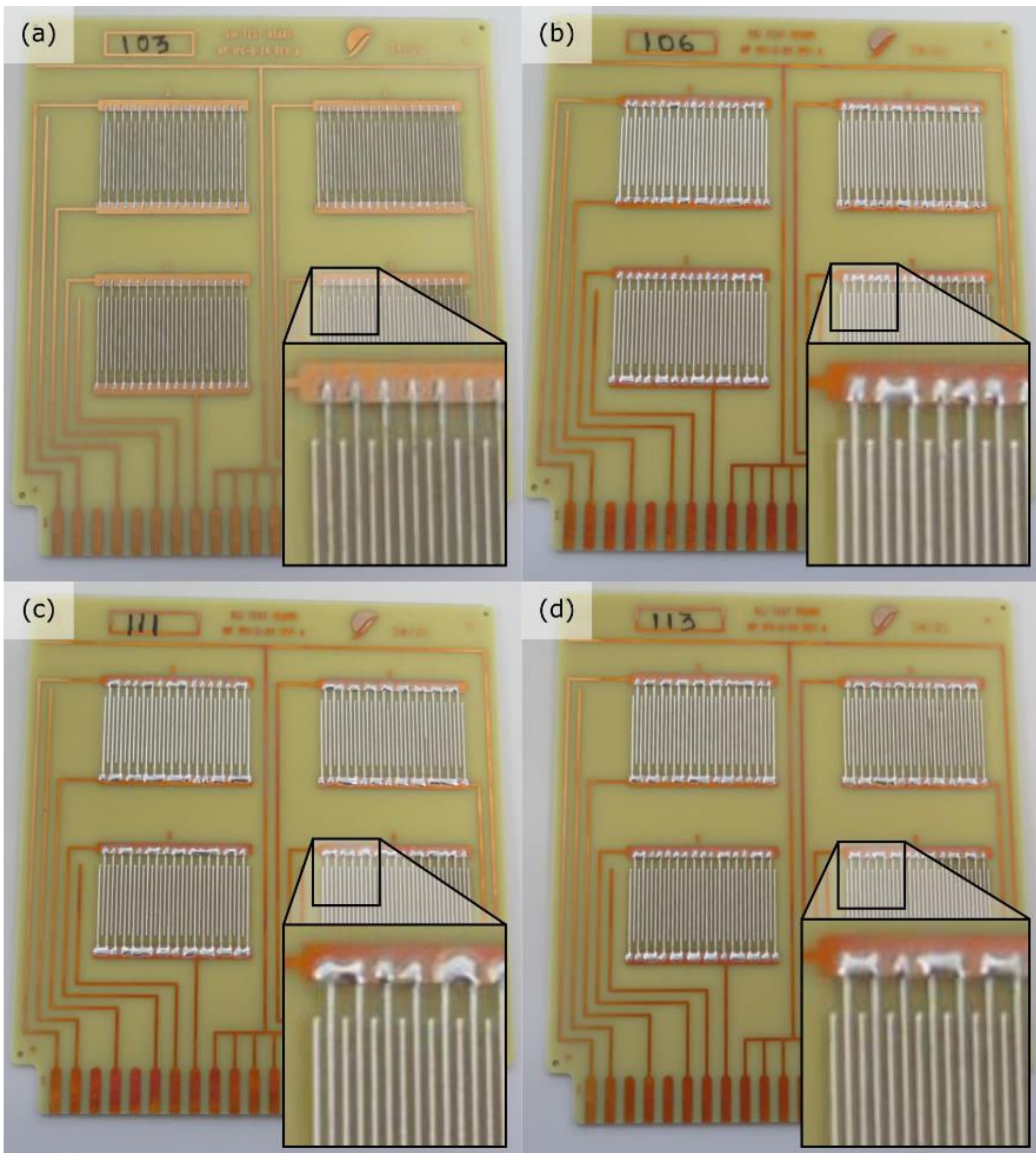

Figure 4. Optical images of SIR test coupons printed with paste "S" and processed using (a) photonic condition 1A, (b) photonic condition 2A, (c) photonic condition 3A, and (d) photonic condition 4A, photographed after SIR testing. Detail views show solder wetting at the bus bar feature for each test coupon pictured.

Incomplete solder coverage at the bus bar features in Figure 4 represents a deviation from the wetting behavior expected from a conventional reflow process, which typically results in full solder coverage over the entirety of bus bar features on the IPC 24-B test coupon. The explanation for this result relates to the time scale of wetting. During reflow, the contact lines of both the liquid flux vehicle and the molten solder advance beyond the original printed area. Whereas, in a conventional reflow process, the solder contact line has sufficient time above liquidus to advance until it achieves a static equilibrium, the cycle time of a photonic reflow process is sufficiently fast that solder re-solidifies before this equilibrium state is reached. This rapid solidification results in an irregular shape of the wetted solder area.

With respect to the SIR results in Figure 3, the wetting behavior of the solder alloy is consequential insofar as it relates to the distribution of flux. During reflow, advancement of the solder contact line is preceded by wetting of the flux vehicle along the copper pad area [15]. Thus, copper areas without solder coverage are likely to be clear of any flux residue as well, particularly when oxidation induced by the reflow process is evident. In Figure 3(b)-(d), darkening of the copper along the bus bar area suggests that this is indeed the case. With relatively little flux residue distributed over the bus bar features, it can be inferred that the difference is made up by the flux residue distributed over the interdigitated fine traces. Crucially, it is the flux residue at the fine trace features that is actually measured by the SIR test, by virtue of the test coupon design [7]. From the fine trace features, the area distribution of flux residue can be reasonably expected to influence the SIR value measured by the IPC J-STD-004B protocol. The influence of dynamic wetting behavior on measured SIR may also explain the variability among individual data series in each subplot of Figure 3(b)-(d). Since the advancement of the solder contact line is not entirely regular, it is possible that the extent of liquid flux egress beyond the interdigitated trace regions, and thus the SIR measured, is stochastic in nature.

The SIR results shown in Figure 4 can be considered a baseline range of SIR performance achievable in a single process cycle. This range is representative because the four conditions used to produce these results are located near two process window boundaries. Specifically, condition 1A is located near the initial onset of solder reflow, while the first process cycle of conditions 2A, 3A and 4A border the onset of discoloration and charring of the FR4 substrate. Similarly, the second process cycles used for conditions 3A and 4A also cover a representative range of the total available process space. The second process cycle for condition 3A constitutes a drying process step that lasts roughly as long as the initial reflow. For condition 4A, the duration of the second process cycle is roughly triple the duration of the reflow step.

These reflow process settings represent only four points within a large and multi-dimensional process space, and it is certainly possible that further improvements to SIR performance can be achieved with further optimizations to cumulative radiant exposure, average radiant power, or pulse shape. However, it should also be appreciated that in practical scenarios, process optimization must also consider the completeness of reflow and wetting at various components on the PCB. These additional requirements can be expected to restrict the process space significantly, which motivates consideration for alternative strategies to improve SIR performance.

Low-Residue Commercial Paste

One possible approach to further SIR improvement is selection of a solder paste that is well-matched to photonic reflow. To explore this approach, additional characterizations were carried out on SIR test coupons printed with solder paste “LR”, which uses a low-residue flux vehicle. SIR results are organized in Figure 5 for each of the four photonic reflow conditions previously listed in Table 2. For test coupons processed under photonic condition 1B, SIR slightly exceeds the 10^8 Ω threshold on average, with slight gradual improvement over the duration of the test, as shown in Figure 5(a). For the remaining photonic conditions whose results are plotted in Figure 5(b)-(d), SIR averages around $10^{10.7}$-$10^{10.8}$ Ω at the start of accelerated lifetime testing, followed by gradual improvement to around $10^{10.9}$-10^{11} Ω at hour 168. The gradual, steady improvement observed across test coupons printed with solder paste “LR” differs from the trends plotted in Figure 3, each of which are characterized by initial SIR drop during the first 15 hours of testing, followed by a gradual recovery until roughly hour 40, and finally, steady SIR performance for the remainder of the test period.

The SIR performance plotted in Figure 5 also differs from the results in Figure 3 in terms of variability across test circuits. For photonic condition 1B results shown in Figure 5(a), SIR values exhibit a narrow spread at hour zero, followed by a steady increase in variability among measurements over the duration of the test. For conditions 2B, 3B and 4B, the initial data spread is much wider, and the range of SIR measurements converges during testing. By contrast, the results for solder paste “S” plotted in Figure 3 exhibit relatively constant spread through the full duration of accelerated lifetime testing.

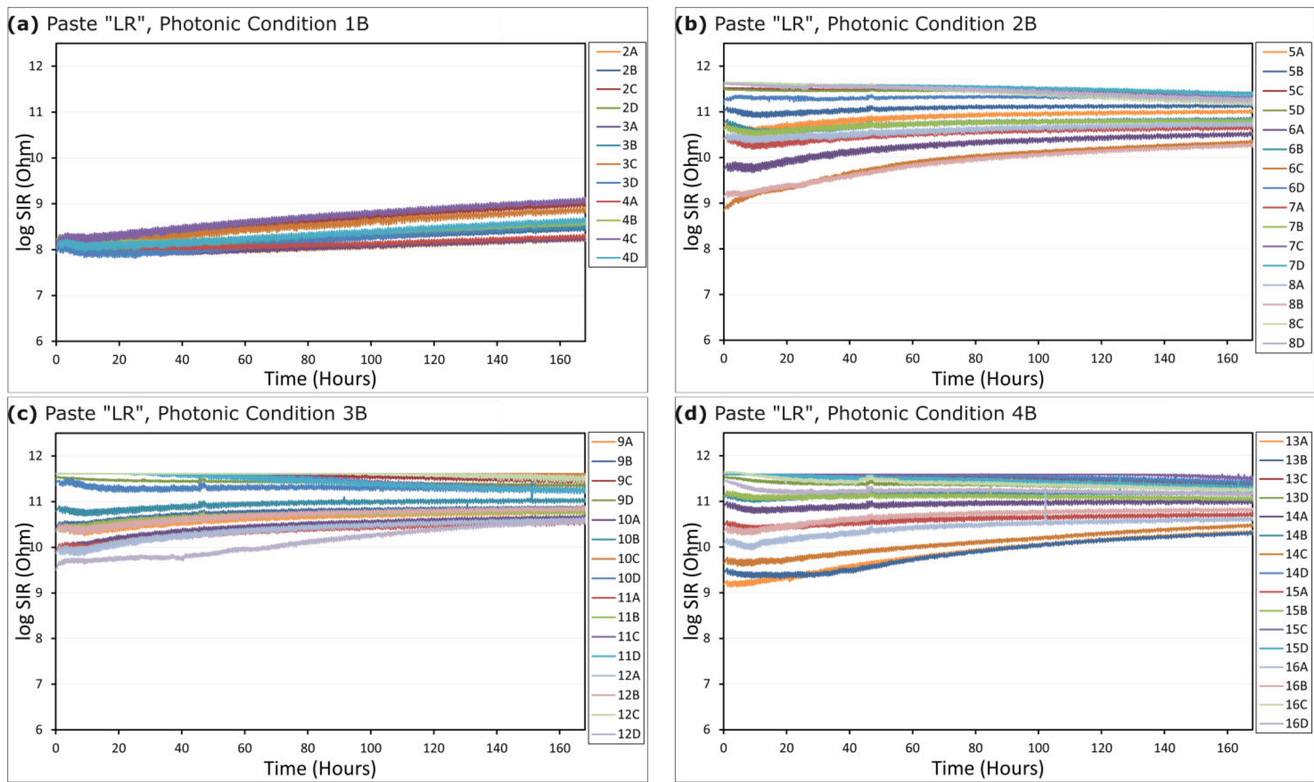

Figure 5. Summary of SIR results for test coupons printed with paste "LR" and processed using (a) photonic condition 1B (b) photonic condition 2B, (c) photonic condition 3B, and (d) photonic condition 4B. Each data series corresponds to a specific SIR test coupon circuit, with four circuits per test coupon. The legend labels of each subplot are the unique identifiers for these circuits.

The SIR measurements for solder paste "LR" in Figure 5 represent over two orders of magnitude improvement versus the performance plotted in Figure 3, and only one order of magnitude lower resistance than that of a control test coupon, whose results are plotted in Figure 6. It should be noted that these data do not necessarily demonstrate any inherent advantage to the flux vehicle used in paste "LR" over the flux vehicle used in paste "S"; rather, the results in Figure 3 and Figure 5 indicate that photonically processed samples benefit significantly by a reduction in flux residue, achieved in this case by means of the solder paste formulation.

Regarding the influence of process conditions on SIR performance, the results for solder paste "LR" largely mirror the previous results for solder paste "S". The initial reflow cycle appears to be far more influential than subsequent low-energy process cycles in determining the measured SIR performance of test coupons. This is reflected in the relatively large difference between results for test coupons processed with photonic condition 1B and the other three conditions, versus nearly identical performance among test coupons processed under photonic conditions 2B, 3B and 4B. As with solder paste "S", it is possible that the flux residue of solder paste "LR" is modified to some degree by the second photonic process cycles in condition 3B and 4B, but that the resulting performance change is too small to be measured by the test equipment.

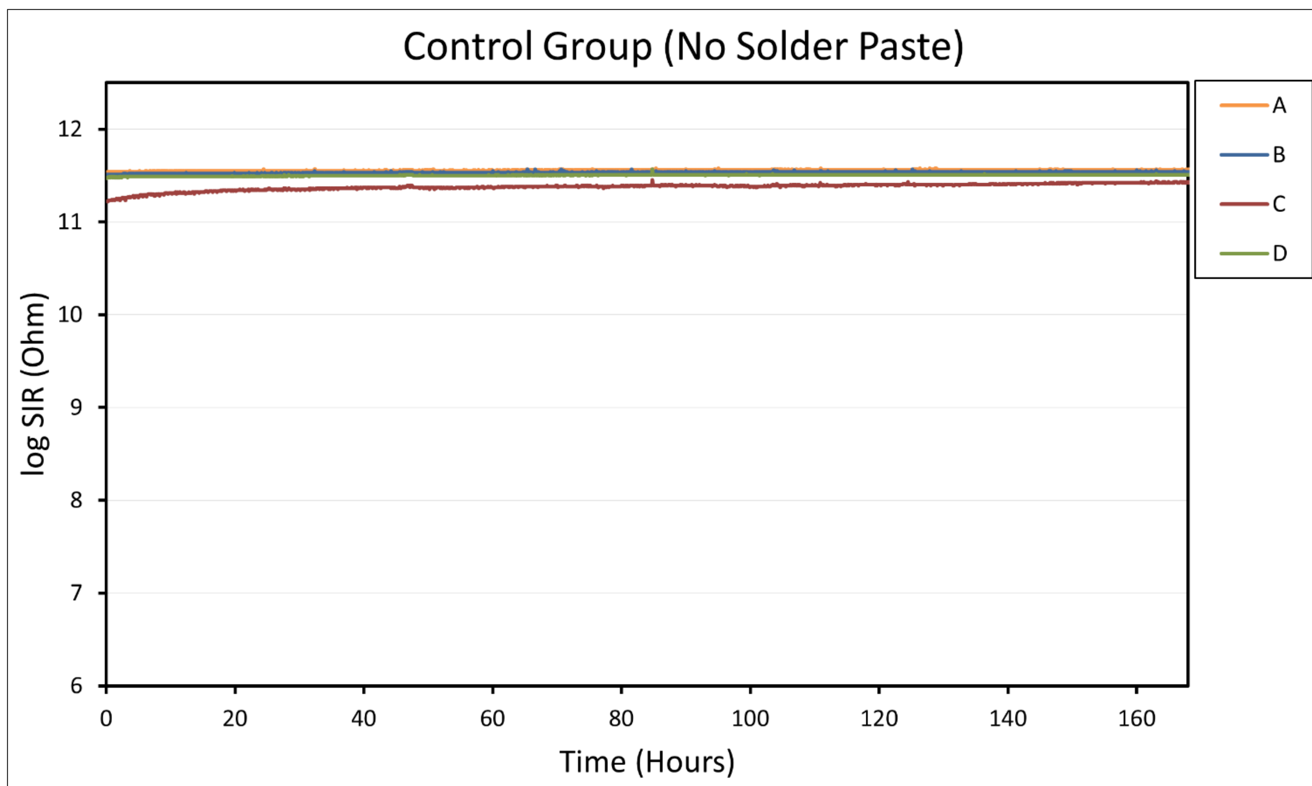

Figure 6. SIR results for a control test coupon, without solder paste printing or reflow processing.

The distribution of solder paste "LR" produced by the photonic conditions in Table 2 provides several insights regarding the physical basis for the results of Figure 3 and Figure 5. Test coupons photonically processed with solder paste "LR", shown in Figure 7, exhibit complete coverage along the fine trace features and partial coverage at the large bus bar features at the top copper layer. For photonic process 1B, the solder contact line is displaced just a few millimeters beyond the initial stencil print area. Solder contact line displacement is largely the same for photonic process conditions 2B, 3B and 4B, in each case several additional millimeters beyond the advancement observed for condition 1B.

In these respects, the wetting behavior of photonically processed test coupons is largely similar for both solder paste types. The explanation for partial coverage along the bus bar feature is therefore the same for both pastes: the photonic reflow cycle is fast compared to more conventional methods, and thus solder coverage is limited by the rate of contact line advancement. Additionally, just as for solder paste "S", one possible explanation for the variability in SIR measured for solder paste "LR" is the stochastic nature of contact line advancement, which introduces a random aspect to the quantity of flux residue distributed over the fine interdigitated copper traces.

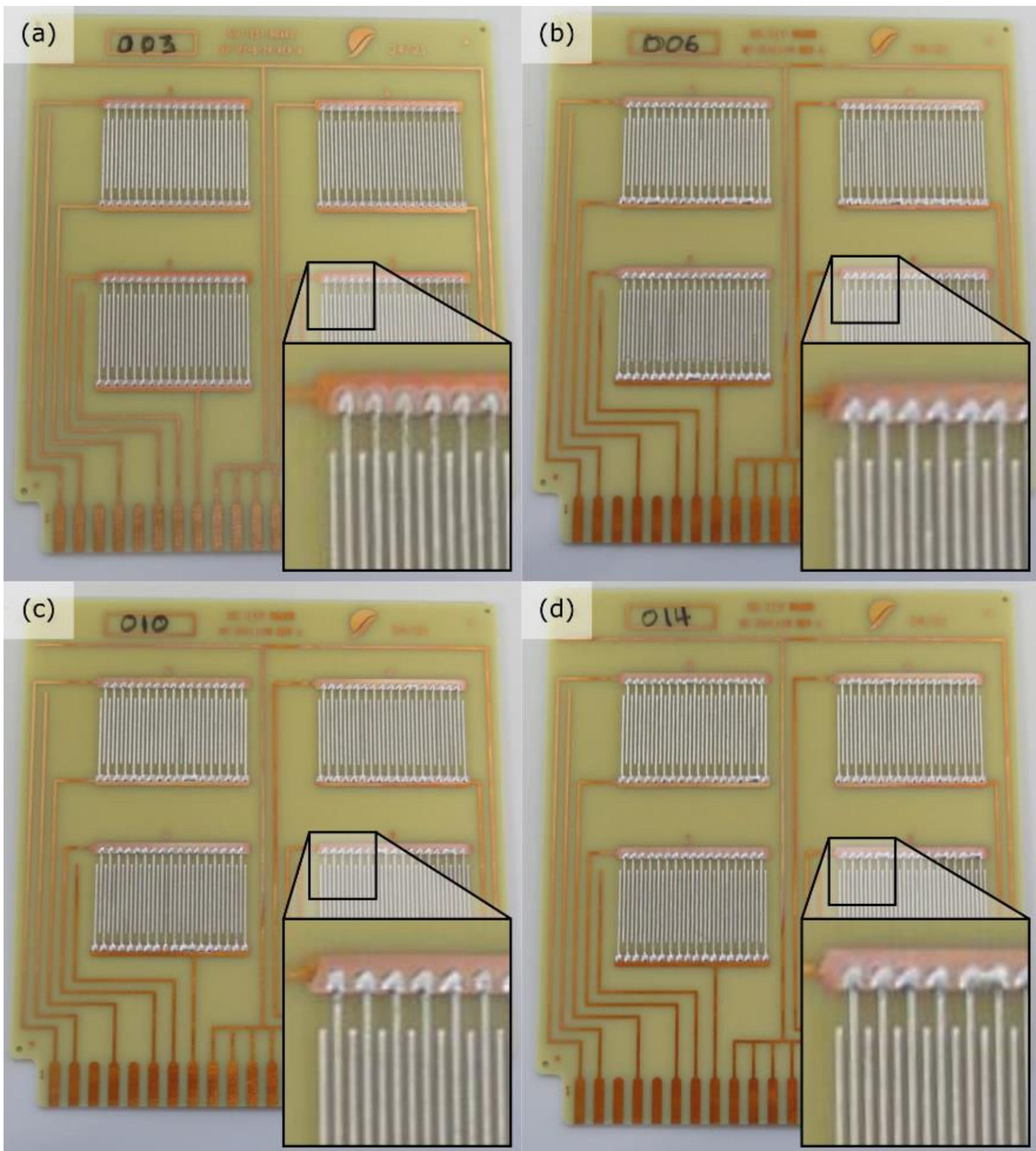

Figure 7. Optical images of SIR test coupons printed with paste "LR" and processed using (a) photonic condition 1B, (b) photonic condition 2B, (c) photonic condition 3B, and (d) photonic condition 4B, photographed after SIR testing. Detail views show solder coverage at the bus bar feature for each test coupon pictured.

Conclusions

The present study has evaluated photonic reflow in terms of SIR performance for two representative no-clean SAC305 pastes, one formulated with a standard flux vehicle, and one formulated with a low-residue flux vehicle. These efforts have yielded several important implications regarding the use of photonic reflow processes for assembly of electronic circuits.

First, ambient oxygen requirements associated with the low-residue paste were shown to be less restrictive with photonic processing than for a standard oven reflow process. The results from this study highlight the inherently fast cycle time of the

339 photonic approach – typically several seconds – as the factor that enables favorable wetting and metallurgical bond formation
340 with paste formulated for <100 ppm O_2 environment, even when processed photonically in ambient air. Second, SIR
341 performance of a photonically processed circuit has been shown to depend on cumulative radiant exposure, which is one of the
342 fundamental parameters that define a photonic process profile. A positive correlation between SIR and cumulative radiant
343 exposure has been observed, and these results suggest that the brevity of the photonic reflow process constitutes a challenge
344 for the removal of volatile compounds from the flux vehicle during reflow. The use of a low-residue paste formulation has been
345 highlighted as one viable route to overcoming this challenge. Finally, the addition of a second photonic process cycle, intended
346 to modify the flux residue composition without additional reflow of the solder paste alloy, has been evaluated as an alternative
347 means to improve SIR performance. This evaluation has produced a null result, although further optimizations of photonic
348 process conditions in conjunction with this strategy have not been ruled out.
349
350 The solder paste formulations considered in this study, along with many solder products available commercially today, were
351 developed originally for conventional reflow processes other than photonic soldering. Consequentially, the validated SIR
352 performance of these pastes must be verified specifically for photonic processing, and while photonic reflow does appear to
353 permit adequate SIR performance for two representative cases, the process conditions of the photonic cycle must be chosen
354 appropriately in order to obtain favorable SIR performance. In the future, solder paste recipes specifically developed for
355 photonic reflow are likely to enable further improvements to SIR performance.
356
357 The use of photonic reflow to limit ambient oxygen activity by means of a rate restriction, rather than a supply restriction, is a
358 compelling possibility arising from this work that merits continued study and application. It may also be worthwhile to consider
359 alternative SIR measurement protocols in future evaluations of photonic reflow, particularly towards a clearer understanding
360 of how distribution of the flux vehicle may affect measured SIR values. Finally, the interplay between reflow cycle duration
361 and the rate of solder contact line advancement illustrated in this study may yet prove consequential for PCB design and paste
362 print optimization.
363
364 **References**

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